Ministerul Educației al Republicii Moldova

Universitate de Stat “A. Russo”

Facultatea de Științe Reale, Economice si ale Mediului

**Raport**

**“Arhitectura și organizarea calculatorului”**

Lucrarea de laborator nr. 9

**Sumatorul**

Student: Sandiuc Vitalie

Grupa: IS21Z

**Scopul lucrării:**

1. Construirea și studierea semisumatorului în regim static și dinamic.

2. Construirea și studierea sumatorului complet.

3. Construirea și studierea sumatorului paralel cu transfer consecutiv al depășirilor.

4. Construirea și studierea sumatorului paralel cu transfer paralel al depășirilor.

**Experimentul nr. 1. Semisumatorul**

**Regim static.**

Tabelul 1. Tabelul de adevăr al semisumatorului

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | S |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Functiile logice ale semisumatorului exprimate prin elemente logice SAU-NU.

C =

S =

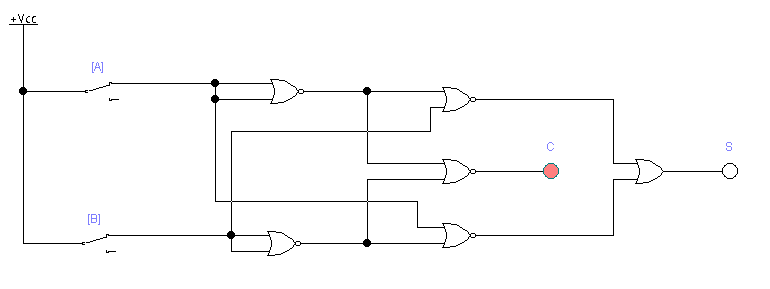
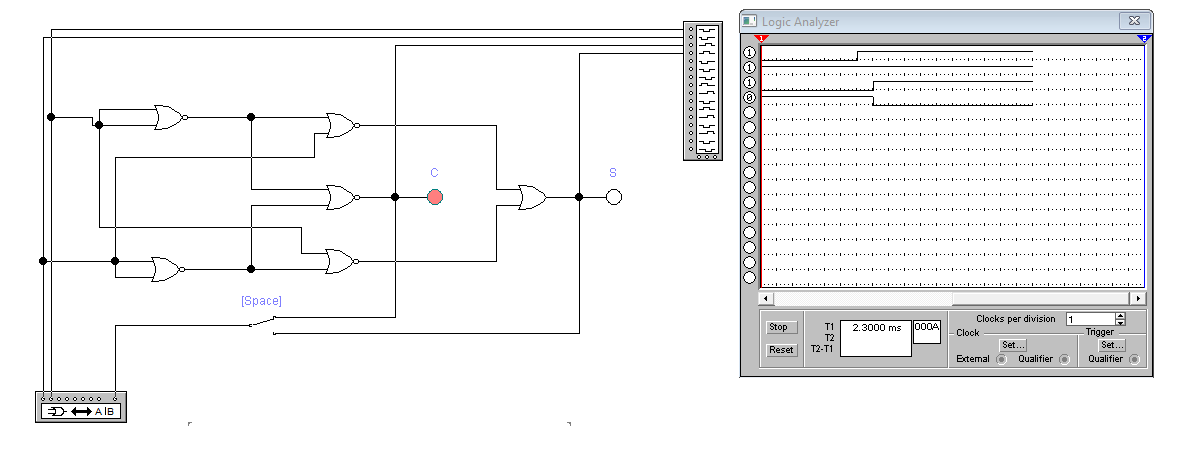


Fig.1. Schema electrica a semisumatorului (regim static)

**Regim dinamic.**



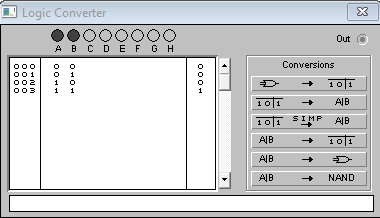
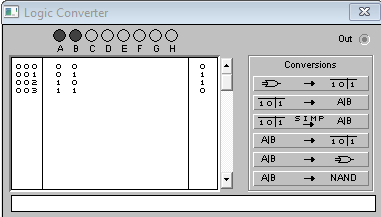
 

Fig. 2. Schema electrică a semisumatorului (regim dinamic).

**Experimentul nr. 2. Sumator complet**

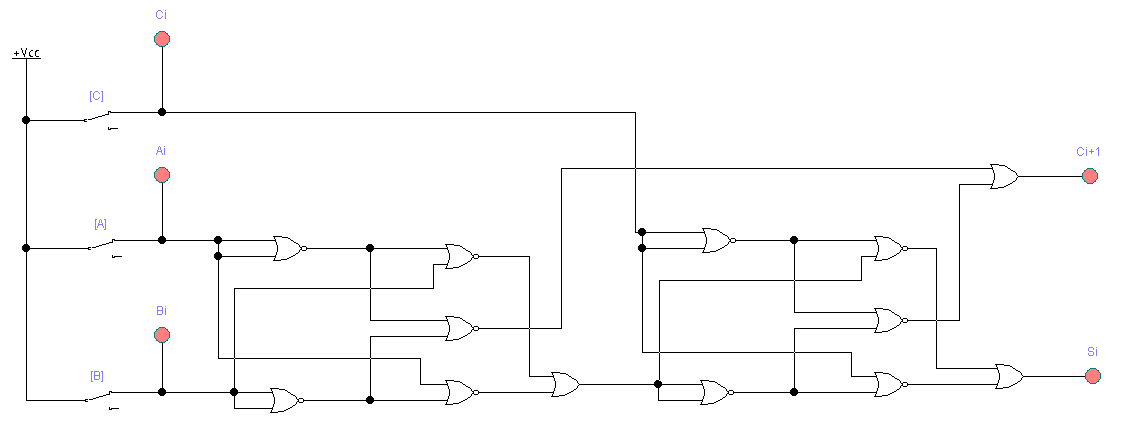
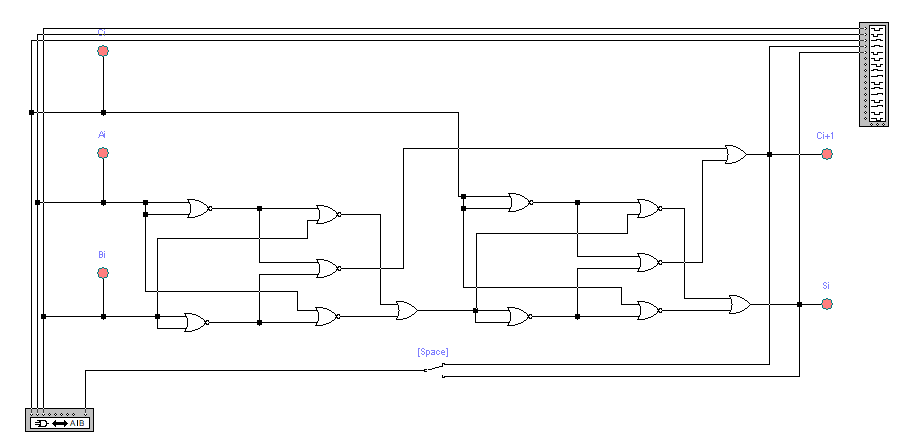


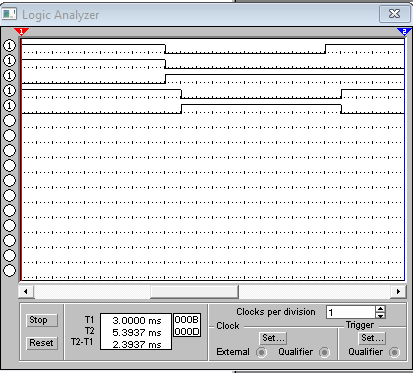
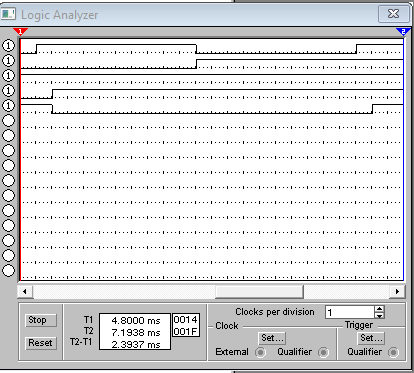
Fig. 3. Schema electrică a sumatorului complet (regim static).

Tabelul 2. Tabelul de adevăr al sumatorului complet

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| C | A | B | Ci+1 | Si |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Regim dinamic.**



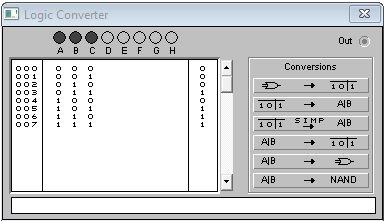
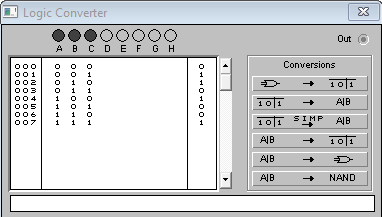
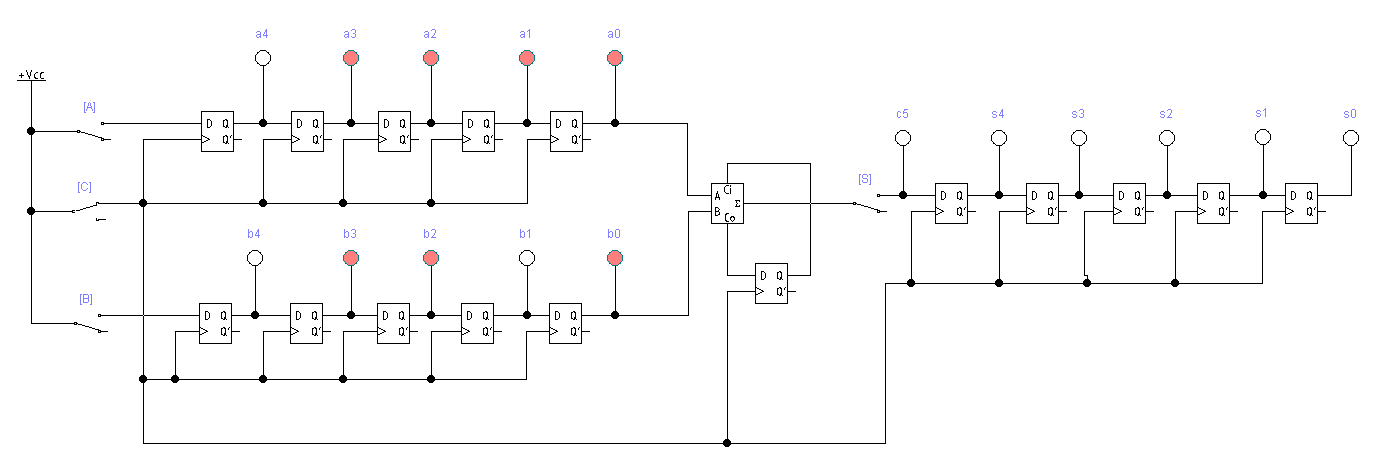
 

Fig. 4. Schema electrică a sumatorului complet (regim dinamic).

**Experimentul nr. 3. Sumator consecutiv**

Tabelul 3. Variante de numere binare

|  |  |  |
| --- | --- | --- |
| Varianta | Numarul A | Numarul B |
| 17 | 01111 | 01101 |



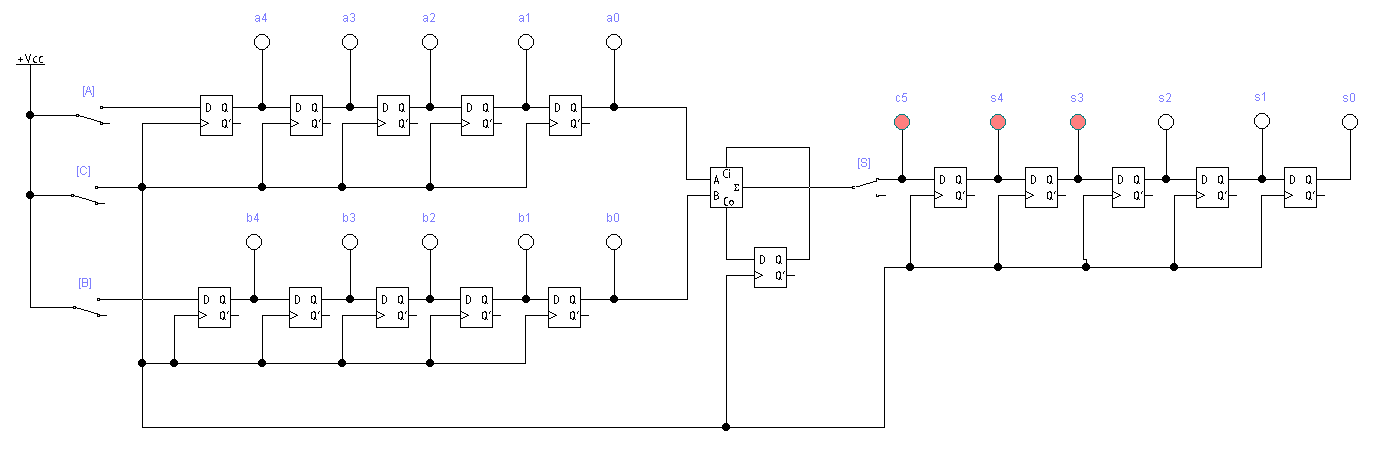


Fig.5. Sumator consecutiv

**Experimentul nr. 4. Sumator paralel cu transfer consecutiv al depășirilor**

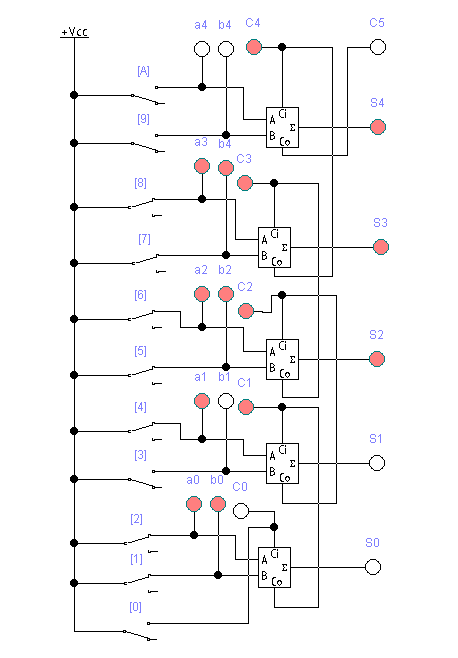


Fig.6. Sumator paralel cu transfer consecutiv al depasirilor

**Experimentul nr. 5. Sumator paralel cu transfer paralel al depășirilor**

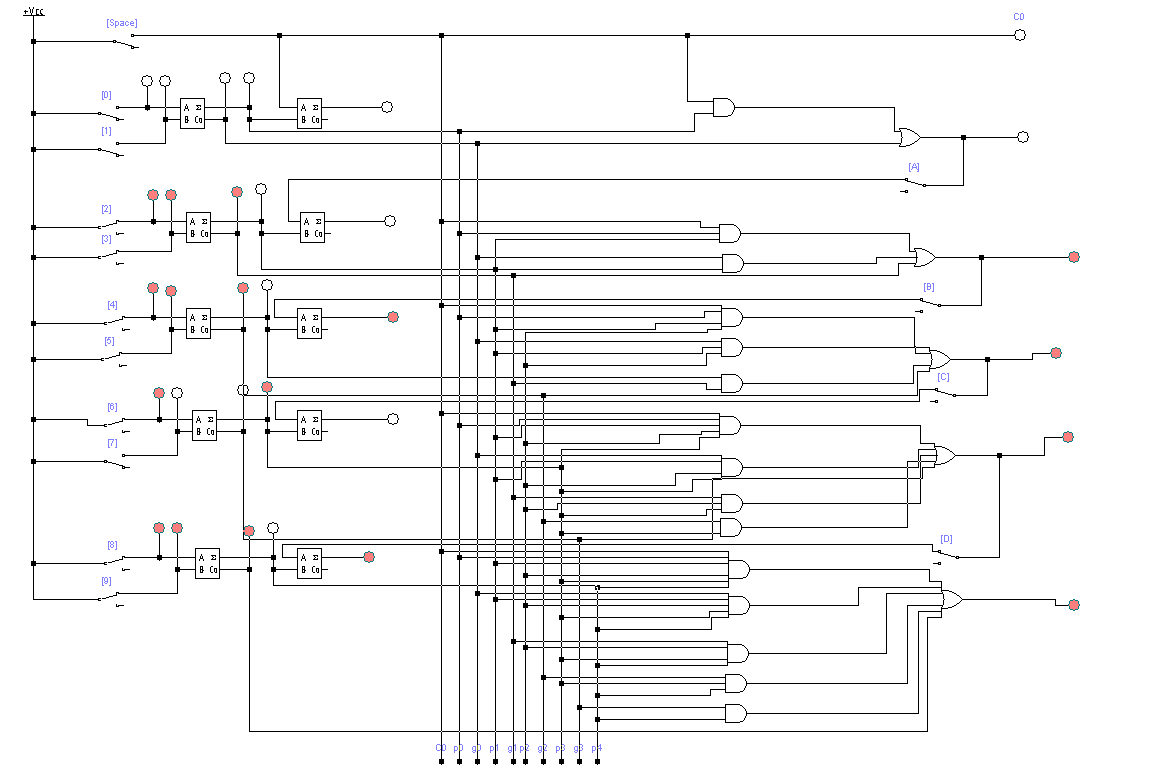


Fig.7. Sumator paralel cu transfer paralel al depasirilor